REMARKS

Claims 1-18 are pending in this application. In this Amendment, the specification has been amended in response to the Examiner's objection to the specification. The specification has also been amended to correct a typographic oversight. Therefore, the present Amendment does not generate any new matter or any new issue for that matter. Accordingly, entry of the present Amendment is solicited pursuant to 37 C.F.R. §1.116.

Claims 1, 7 and 13 have been rejected under 35 U.S.C. §103(a) as being anticipated by Augusteijn et al.

Applicant argued in the July 8, 2005 response that Augusteijn et al. does not disclose the select circuit in claims 1 and 7, and the selectively applying step in claim 13. The Examiner responded that DET 440 in Fig. 4 of the reference corresponds to the claimed select circuit and performs the same step as the selectively applying step. Reconsideration of this position is solicited. The claims are distinguishable from DET 440 as discussed below.

Claims 1, 7 and 13 require "selectively applying the information read from said external memory space and the instruction prepared by the translation of the instruction read from said external memory space to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not." The claimed invention provides the information (including a nonnative instruction, a native instruction and data), or the instruction translated from the nonnative instruction, to the processor core depending on where such information or instruction is fetched.

On the other hand, what DET 440 does is to detect whether or not conversion of an instruction is required (native instruction need not be converted) and which conversion means

should be used for the conversion (see column 6, lines 4-8 of Augusteijn et al.; and paragraph 7 of the Office Action). However, DET 440 is not configured to select a non-converted instruction or a converted instruction, and apply the selected one to microprocessor core 114. Therefore, the claimed select circuit and DET 440 of Augusteijn et al. are different from each other.

The above-described fundamental differences between the claimed invention and Augusteijn et al. undermine the factual determination that Augusteijn et al. identically describes the claimed invention within the meaning of 35 U.S.C. §102. Applicant, therefore, submits that the imposed rejection of claims 1, 7 and 13 under 35 U.S.C. §102(e) for lack of novelty as evidenced by Augusteijn et al. is not factually viable and, hence, respectfully solicits withdrawal thereof.

Claims 1, 7 and 13 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Arya in view of Hammond et al.

Applicant's previous arguments were that the applied combination does not teach the claimed select circuit. Specifically, Applicant argued that demultiplexer 540 of Hammond et al. does not select translator 541 or instruction cache 520 "depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not" (see claims 1, 7 and 13).

In response, the Examiner asserted that demultiplexer 540 selects translator 541 or instruction cache 542 based on jmpx and x86jmp instructions associated with a target address (see paragraph 40 of the Office Action). Even if this assertion were assumed to be correct, Hammond et al. does not teach, at a minimum, the claimed select circuit.

The claimed select circuit is configured to select "the information read from said external memory space" (including a non-converted instruction) or "the instruction prepared by translating the instruction read from said external memory space." On the other hand, demultiplexer 540 of Hammond is configured to select translator 541 or instruction cache 542, but not configured to select a non-converted instruction or a converted instruction. Accordingly, there is a difference between the claimed invention and the applied combination of the references. The claimed invention would not have been suggested by a consideration of the references, taken individually or collectively.

Based upon the foregoing, Applicant submits that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention for lack of the requisite factual basis. Applicant, therefore, submits that the imposed rejection of claims 1, 7 and 13 under 35 U.S.C. §103 for obviousness predicated upon Arya in view of Hammond et al. is not factually or legally viable and, hence, respectfully solicits withdrawal thereof.

Claims 2-6, 8-12 and 14-18 have been rejected under 35 U.S.C. §103(a).

Claims 2-4, 8-10 and 14-16 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Augusteijn et al. in view of IBM Technical Disclosure Bulletin, NN610843 ("IBM TDB"); claims 5, 11 and 17 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Arya in view of Hammond et al. and further in view of Denman et al.; and claims 6, 12 and 18 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Arya in view of Hammond et al. and further in view of Jouppi.

In response, it is submitted that claims 2-6, 8-12 and 14-18 are patentably distinguishable over the cited references at least because the claims respectively include all the limitations

recited in independent claims 1, 7 and 13. IBM TDB, Denman et al. and Jouppi do not teach the claimed invention in independent claims 1, 7 and 13, and thus, do not cure the deficiencies of Augusteijn et al. and the applied combination of Arya and Hammond et al.

Applicant, therefore, respectfully solicits withdrawal of the rejection of claims 2-6, 8-12 and 14-18 under 35 U.S.C. §103(a), and favorable consideration thereof.

Conclusion

As claims 1-18 are patentably distinguishable from the applied references, withdrawal of the imposed rejections is appropriate. Allowance of the application, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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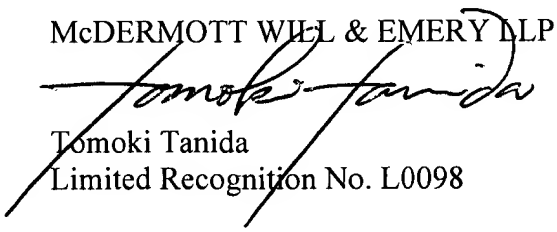

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